IN THE SPECIFICATION:

On page 1 of the Specification, please insert the following sections after the Title and before the Background Of The Invention:

INVENTORS

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CROSS-REFERENCE TO RELATED APPLICATIONS

The present application is a divisional of U.S. Application Serial No. 09/687,787 entitled THIN AND HEAT RADIANT SEMICONDUCTOR PACKAGE AND METHOD FOR MANUFACTURING filed October 13, 2000.

On page 1, line 5 of the Specification, please amend the caption as follows:

[~~TECHNICAL~~] FIELD OF THE INVENTION

Please amend the passage of the Specification beginning on page 3, line 10 and ending on page 3, line 19 as follows:

BRIEF SUMMARY OF THE INVENTION

In one embodiment of the present invention, there is provided a semiconductor package comprising a semiconductor chip having an upper surface and a bottom surface. A plurality of input bonds pads and output bond pads on the upper surface of the semiconductor chip and along the [~~circumference~~] **perimeter** of the semiconductor chip are electrically connected to the semiconductor chip. A chip paddle may be provided which has a top surface, a side surface and a bottom surface. The chip paddle is bonded to the bottom surface

of the semiconductor chip by an adhesive. The chip paddle has corners, a [~~circumference~~] **perimeter** and a half-etched section at the lower edge of the chip paddle along the chip paddle [~~circumference~~] **perimeter.**

Please amend the passage of the Specification beginning on page 3, line 25 and ending on page 3, line 35 as follows:

A plurality of internal leads connect to the leadframe. Each of the leads has a side surface and a bottom surface. The leads are radially formed at regular intervals along and spaced apart from the [~~circumference to~~] **perimeter of** the chip paddle and extend towards the chip paddle. Each of the leads has a step shaped half-etched section facing the chip paddle.

A plurality of via conductive wires are electrically connected to and between the plurality of leads and the semiconductor chip. Encapsulating material encapsulates the semiconductor chip, conductive wires, chip paddle, and the leads to form a package body. The flow of the encapsulation material is limited by the dam bars formed on the leadframe. The dam bars also serve to stabilize the leads on the leadframe. After encapsulation, the chip paddle, leads, and tie bars are externally exposed at respective [~~side and~~] bottom **and side** surfaces.

Please amend the passage of the Specification beginning on page 4, line 11 and ending on page 4, line 13 as follows:

A more complete understanding of the method and apparatus of the present invention may be obtained by reference to the following detailed description, **with like reference numerals corresponding to like elements,** when taken in conjunction with the accompanying Drawings wherein:

Please amend the passage of the Specification beginning on page 4, line 28 and ending on page 5, line 11 as follows:

DETAILED DESCRIPTION OF THE ~~[PREFERRED EMBODIMENTS]~~ **INVENTION**

Referring first to FIG. 1A and 1B, there is shown a cross-sectional illustration of one embodiment of ~~[a]~~ semiconductor package**s** 10**, 11 respectively,** construed in accordance with the principles of the present invention. The semiconductor package**s** 10**, 11** include~~[s]~~ a corner 12 and bottom surface 15. The semiconductor package**s** 10**, 11** further include~~[s]~~ a semiconductor chip 20 having an upper surface 30, a ~~[circumference]~~ **perimeter** 40 and a bottom surface 50. A plurality of input bond pads 60 and output bond pads 70 are disposed on the upper surface 30 of the semiconductor chip 20. Conductive wires 75, including but not limited to gold or aluminum wires, electrically connect the semiconductor chip 20 to the respective input bond pads 60 or output bond pads 70.

In an alternate embodiment **of semiconductor packages 12, 13** best seen in FIG. 2A and 2B, **respectively,** a chip paddle 80 having a**n** upper surface 90, a side surface 100 and a bottom surface 110 is secured to the bottom surface 50 of the semiconductor chip 20 via an adhesive 120. The chip paddle 80 has corners 130, a ~~[circumference]~~ **perimeter** 140 and may include a half-etched section 150. The half-etched section 150 is located at a lower edge 160 of the chip paddle 80.

Please amend the passage of the Specification beginning on page 5, line 16 and ending page 6, line 35 as follows:

A plurality of leads 230 are connected to the leadframe 170 and have an upper surface 235, a side surface 240 and a bottom surface 250 **(FIGS. 1A and 2A)**. In a first embodiment seen in FIGS. 1A and 1B, the leads 230 are radially formed at regular intervals along the semiconductor chip ~~[circumference]~~ **perimeter** 40 and spaced apart from the ~~[circumference]~~ **perimeter** 40 of the semiconductor chip 20. The leads 230 extend towards the **semiconductor** chip 20 and have a half-etched section 260 facing the **semiconductor** chip 20.

In an alternate embodiment best seen in FIGS. 2A and 2B, the leads 230 are radially formed at regular intervals along the chip paddle ~~[circumference]~~ **perimeter** 140 and spaced apart from the ~~[circumference]~~ **perimeter** of the chip paddle 80. The leads 230 extend towards the chip paddle 80, such that each of the plurality of leads 230 has a half-etched section 260 facing the chip paddle 80.

Referring back to FIGS. 1B and 2B, there is shown a ground ring 262 formed in **the semiconductor** package**s** ~~[10]~~,**11, 13.** The ground ring 262 is positioned between the semiconductor chip 20 and the plurality of leads 230, and may be interchangeably used as a power ring should circumstances require. Conductive wires 75 can connect the ground ring 262 to the respective input bond pads 60 or output bond pads 70, depending on the application. As seen in FIG. 1B, the upper surface 264 of the ground ring 262 is planar with the upper surface 30 of the semiconductor chip 20 and the upper surface 235 of the leads 230. However, as seen in FIG. 2B, the upper surface 264 of the ground ring 262 may be planar with the upper surface of the chip paddle 80 to minimize package thickness. Likewise, the upper surface 235 of the leads 230 is planar with the upper surface 30 of the semiconductor chip 20 (FIGS. 1A and 1B) to minimize package thickness. In the alternate embodiments shown in FIGS. 2A and 2B, the upper surface 235 of the leads 230 is planar with the upper surface 90 of the chip paddle 80 to reduce package thickness.

Referring generally now to FIGS. 1A and 3, ~~[to enclose]~~ the semiconductor ~~[package 10,]~~ **chip 20 and leads 230 are partially encapsulated with an** encapsulation material 280 ~~[at least partially encapsulates]~~ **to form a semiconductor package body in which** the semiconductor chip 20 ~~[conductive wires 70,]~~ and leads 230 **are exposed directly to the outside at their respective bottom surfaces 50, 250.** In the alternate embodiment shown in FIG. 2A and 2B, the ~~[encapsulation material 280 encapsulates the]~~ chip paddle 80 ~~[as well]~~ **is also encapsulated by the encapsulation material 280. In this alternate embodiment, the bottom surfaces 250, 110 of the leads 230 and chip paddle 80 are directly exposed to the outside.** Likewise, for the embodiments shown in FIGS. 1B and 2B, the ~~[encapsulation material 280 encapsulates]~~ **leads 230, semiconductor chip 20, and ground rings 262 are partially encapsulated to form a semiconductor package body in**

which the bottom surface 266 of the ground ring 262 **is also exposed to the outside of the semiconductor package body.**

Referring now to FIGS. 1 through 3 in general, dam bars 220 limit the flow of the encapsulation material 280 on the leadframe 170 and provide stability to the leads 230 on the leadframe 170. In the respective embodiment during encapsulation, the chip paddle 80, leads 230, and tie bars 180 may be externally exposed at peripheral side and bottom surfaces. The externally exposed portions of chip paddle 80, leads 230, and tie bars 180 may, but do not necessarily have to be, electroplated with corrosion minimizing materials such as but not limited to, tin lead, tin, gold, nickel palladium, tin bismuth, or any other similar material known in the art. The respective half-etched sections 150, 260 of the chip paddle 80 and leads 230 are provided to increase the bonding strength of the encapsulation material 280 in the **respective semiconductor** package**s** 10**, 11, 12, 13.** It is contemplated that the respective half-etched sections 150, 260 may be eliminated without departing from the scope and spirit of this invention.

Referring now to FIGS. 4-9 in general, there is shown a cross-section of the semiconductor package 10 of FIG. 1A. It is to be recognized that the method for constructing the semiconductor package 10 of FIG. 1A may be used for constructing the embodiment shown in FIG. 1B without departing from the principles of this invention. The leadframe ~~[, although not shown in these figures,]~~ having leads 230 and a space 290 large enough to accommodate a semiconductor chip 20, is first placed upon an adhesive tape 300 **(FIG. 4)**. Next, a semiconductor chip 20 is fixed to the adhesive tape 300 within the space 290 as best seen in FIG. 5. The semiconductor chip 20 and leads 230 are pressurized downwardly onto the tape 300 at a suitable temperature to make the tape 300 firmly adhere to the semiconductor chip 20 and leads 230.

Please amend the passage of the Specification beginning on page 7, line 11 and ending on page 9, line 10 as follows:

The semiconductor chip 20, conductive wires 75, and leads 230 are then at least partially encapsulated with the encapsulation material 280, which may be an epoxy molding

compound or a liquid encapsulation material, thereby forming a **semiconductor** package ~~[body]~~ 10 as seen in FIG.7. Referring to FIG.8, the adhesive tape 300 is next removed from the bottom surface 15 of the **semiconductor** package 10. The leads 230 are next severed from the leadframe (not shown) by cutting through the dam bars (not shown) or neighboring areas of the **semiconductor** package ~~[body]~~ 10 best seen in FIG.9 as a singulation step. It is to be noted that this singulation step may occur before the adhesive tape 300 is removed.

After the formation of the **semiconductor** package ~~[body]~~ 10, a marking process (not shown) may be carried out by the use of ink or lasers. The removal of the adhesive tape 300 allows the semiconductor chip 20 and leads ~~[240]~~ **230** to be exposed to the outside, thereby improving heat radiation. By adhering the adhesive tape ~~[250]~~ **300** to the bottom **surface 15 of the semiconductor package 10, which includes bottom** surfaces ~~[15]~~ **50**, 250 of the semiconductor chip 20 and leads 230, respectively, flashes, which are typically formed during the molding process are not generated, thereby eliminating or reducing any further deflashing steps.

After the removal of the adhesive tape 300, a predetermined thickness of solder (not shown) may be plated over the bottom surface 250 ~~[of the]~~ of the leads 230 to allow easy ~~[fusion]~~ **connection** of the **semiconductor** package 10 ~~[to]~~ **with** a motherboard (not shown).

Referring now generally to FIGS. 10-14, there are shown cross-sections of the semiconductor package ~~[10]~~ **12** of FIG. 2A during various stages of construction. It is to be recognized that the method for constructing the semiconductor package ~~[10]~~ **12** of FIG. 2A may be used for constructing the embodiment shown in FIG. 2B without departing from the principles of this invention. The leadframe (not shown) having leads 230 and a chip paddle 80 is first placed upon an adhesive tape 300 best seen in FIG. 10. The chip paddle 80 and the leads 230 are pressurized downwardly onto the tape 300 at a suitable temperature to make the tape 300 firmly adhere to the chip paddle 80 and leads 230.

As shown in FIG. 11, the semiconductor chip 20 is bonded to the upper surface 90 of the chip paddle 80 via an adhesive 120. The input **bond** pads 60 and output **bond** pads 70 of the semiconductor chip 20 are next electrically connected to the leads 230 via conductive wires 75. Upper surfaces 235 of leads 230 may, but do not necessarily have to be, electroplated with a material that enhances electrical conductivity such as, for example, gold

or silver. Typically, the conductive wires 75 are connected via an automated process, but may also be connected in any alternate method in the industry.

~~[The]~~ **As illustrated in FIG. 12, the** semiconductor chip 20, chip paddle 80, conductive wires 75, and leads 230 are then at least partially encapsulated with the encapsulation material 280, which may be thermoplastics or thermoset resins, with thermoset resins including, for example, silicones, phenolics, and epoxies. The encapsulation material 280 forms a **semiconductor** package ~~[body 10 as seen in FIG.12]~~ **10.**

Referring to FIG. 13, the adhesive tape 300 is next removed from the bottom surface 15 of the **semiconductor** package ~~[10]~~ **12.** The leads 230 are next severed from the leadframe (not shown) by cutting through the dam bars (not shown) or neighboring areas of the **semiconductor** package ~~[body 10]~~ **12** best seen in FIG. 14 in a singulation step. It is noted that this singulation step may occur before the adhesive tape 300 is removed.

Once the **semiconductor** package ~~[body 10]~~ **12** is formed, a marking process (not shown) may be carried out by the use of ink or lasers. The removal of the adhesive tape 300 allows the chip paddle 80 and leads 230 to be exposed to the outside, thereby improving heat radiation. By adhering the adhesive tape 300 to the bottom surfaces 110, 250 of the chip paddle 80 and leads 230, respectively, flashes, which are typically formed during the molding process, are not generated, thereby eliminating or reducing any further deflashing steps. Bottom surfaces 110, 250 of the chip paddle 80 and leads 230, may be electroplated with corrosion-minimizing materials such as, but not limited to, tin lead, tin, gold, nickel palladium, tin bismuth, or other similar materials known in the art.

After the removal of the tape 300, a predetermined thickness of solder (not shown) may be plated over the bottom surface 250 ~~[of the]~~ of the leads 230 to allow easy ~~[fusion]~~ **connection** of the **semiconductor** package ~~[10]~~ **12** ~~[to]~~ **with** a motherboard (not shown).

In such a semiconductor package as described and shown in FIGS. 1A and 1B, the bottom surface 15 of the semiconductor ~~[chip 20]~~ **packages 10, 11** is in the same plane as the bottom surface 250 of the leads 230, so that the semiconductor package**s** 10, **11** [~~is~~] **are** thin by limiting the height level of the conductive wires 75. In addition, the direct exposure of the semiconductor chip 20 provides for higher thermal radiation.

The following applications are all being filed on the same date as the present application and all are incorporated by reference as if wholly rewritten entirely herein:

Attorney Docket No.	**Title of Application**	**First Named Inventor**
~~[45475-00014]~~ **09/687,331**	Lead Frame for Semiconductor Package and Mold for Molding the Same	Young Suk Chung
~~[45475-00017]~~ **09/687,532**	Method for Making a Semiconductor Package Having Improved Defect Testing and Increased Production Yield	Tae Heon Lee
~~[45475-00018]~~ **09/687,876**	Near Chip Size Semiconductor Package	Sean Timothy Crowley
~~[45475-00022]~~ **09/687,536**	End Grid Array Semiconductor Package	Jae Hun Ku
~~[45475-00026]~~ **09/687,048**	Leadframe and Semiconductor Package with Improved Solder Joint Strength	Tae Heon Lee
~~[45475-00027]~~ **09/687,585**	Semiconductor Package Having Reduced Thickness	Tae Heon Lee
~~[45475-00029]~~ **09/687,541**	Semiconductor Package Leadframe Assembly and Method of Manufacture	Young Suk Chung
~~[45475-00030]~~ **09/687,049**	Semiconductor Package and Method Thereof	Young Suk Chung